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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PATEL, ANAND B	
ART UNIT	PAPER NUMBER
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/648,198	YANG, PACHINCO	
	Examiner	Art Unit	
	Anand Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Request for Continued Examination filed 12/15/06 has been entered and as such claim 1 has been amended.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 10, 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No 6005180 to Masuda in view of US Patent No 6643843 to Reger.

- As per claim 1, Masuda discloses a data processing system (figure 1) comprising:
  - A non-volatile program memory (2) for storing a startup program (column 3, lines 65-66);
  - A volatile memory (3) for storing programs or data temporarily (column 3, line 66 – column 4, line 1);
  - A permanent memory (4) for storing an application program permanently (column 4, lines 1-7);
  - A bus (BUS LINE) connected to the microprocessor, the volatile memory, and the permanent memory for transmitting programs or data (column 3, lines 63-65); and
  - A power supply comprising a switch and providing power to the data processing system to maintain normal operation of the data processing system (inherent given system startup in figure 4 and column 6, lines 40-42);
  - Wherein, while the switch of the power supply is turned on, the startup program stored in the non-volatile program memory is initialized first to load the application program from the

permanent memory into the volatile memory via the bus, so that the CPU only needs to call and execute the application program in the volatile memory, instead of the permanent memory (column 6, lines 40-52).

Masuda fails to disclose a microprocessor. Reger teaches a microprocessor comprising a CPU for executing programs or calculating data (12) and a non-volatile program memory (24) wherein the non-volatile program memory and the CPU are on-chip built-in within the same microprocessor package (column 3, lines 45-48). An advantage of the system taught by Reger is the ability to reliably, quickly, and cost-effectively update program memory (column 2, lines 55-57). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Masuda with the microprocessor as taught by Reger. Motivation to modify is to cut costs and improve updating procedures.

- As per claim 10, Masuda discloses a data processing system wherein the permanent memory is used for storing the application program and is provided for the CPU to access data (column 4, lines 1-7).
- As per claim 15, Masuda discloses a data processing system wherein while the switch of the power supply is turned off, the application program stored in the volatile memory vanishes (inherent given that RAM is a volatile memory); however, the startup program stored in the non-volatile program memory and the application program stored in the permanent memory are kept (inherent given that ROM and hard drives are nonvolatile memories).
- As per claim 16, Masuda discloses a data processing system wherein the data processing system does not comprise an external non-volatile program memory for storing the application program (figure 1).

4. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda in view of Reger and US Patent No 6668266 to Kiuchi et al (Kiuchi).

- As per claim 2, Reger teaches wherein the non-volatile program memory is a ROM (24). Masuda and Reger fail to disclose a mask ROM. Kiuchi teaches a mask ROM as a type of ROM (column 6, lines 35-38). An advantage of the system taught by Kiuchi is the ability to enhance efficiency of a data processing system (column 2, lines 30-48). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Masuda and Reger to include the mask ROM as taught by Kiuchi. Motivation to modify is to increase system efficiency.
- As per claim 3, Reger teaches wherein the non-volatile program memory is a ROM (24). Kiuchi teaches a flash memory as a type of ROM (column 6, lines 35-38).

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda in view of Reger and US Patent No 4745392 to Ise et al (Ise).

- As per claim 4, Reger teaches a non-volatile program memory (24). Masuda and Reger fail to disclose specific capacities of the memory. Ise teaches a read-only memory that is 1 kilobyte (column 5, lines 26-31). An advantage of the system taught by Ise is the ability to reduce noise in signal transmission (column 1, lines 18-33). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Masuda and Reger to include the read-only memory with a 1kb size as taught by Ise. Motivation to modify is to reduce noise in signal transmissions.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda in view of Reger and US Patent No 6314024 to Kakihara.

- As per claim 5, Masuda discloses a data processing system with an application program (OS). Masuda and Reger fail to disclose specific sizes of the programs. Kakihara teaches a program that is between 32K and 1M bytes (column 5, lines 25-27), and is larger than the capacity of the non-volatile program memory (inherent given the ROM is 1 kilobyte). An advantage of the system taught by Kakihara is the ability to easily correct bugs in a program (column 2, lines 10-15). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Masuda and Reger

to include the program of size between 32K and 1Mbytes as taught by Kakihara. Motivation to modify is to more easily remedy program flaws.

7. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda in view of Reger and US Patent No 6832194 to Mozer et al (Mozer).

- As per claim 6, Masuda discloses a data processing system with a volatile memory (3). Masuda and Reger fail to disclose specifics of the memory. Mozer teaches a volatile memory that is a built-in static random access memory (SRAM) inside the microprocessor (column 14, lines 29-32). An advantage of the system taught by Mozer is the ability to implement a processing system with lower costs and higher flexibility (column 1, line 60 – column 2, line 1). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Masuda and Reger to implement the memory as a static random access memory built into the microprocessor as taught by Mozer. Motivation to modify is to lower costs and increase flexibility.
- As per claim 7, Masuda discloses a data processing system with a volatile memory (3). Mozer teaches a volatile memory that is an external dynamic random access memory (DRAM) outside the microprocessor (column 14, lines 29-32).

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda in view of Reger and US Patent No 5701511 to Smith.

- As per claim 8, Masuda discloses a data processing system with a volatile memory (3). Masuda and Reger fail to disclose specifics of the memory. Smith teaches a volatile memory that is used for temporarily storing the temporary data generated by the application program and the CPU (column 4, lines 55-58). An advantage of the system taught by Smith is the ability to synchronize various data streams at lower costs (column 2, lines 9-18). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Masuda and Reger to use the memory to temporarily store

temporary data generated by the application program and the CPU as taught by Smith. Motivation to modify is to lower costs in the system.

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda in view of Reger and US Patent No 6683817 to Wei et al (Wei).

- As per claim 9, Masuda teaches a permanent memory that is a hard drive external to the microprocessor (4; figure 1). Masuda and Reger fail to disclose specifics of the memory. Wei teaches equivalence of a NAND flash memory and a hard disk (column 7, lines 63-66). An advantage of the system taught by Wei is the ability to improve data transfer and data integrity (column 2, lines 5-9). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Masuda and Reger to substitute the hard disk with the NAND flash memory as taught by Wei. Motivation to modify is to improve data transfer performance and data integrity.

10. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda in view of Reger and Applicant's Admitted Prior Art (AAPA).

- As per claim 11, Masuda and Reger fail to disclose wherein the data processing system is a digital still camera. AAPA teaches wherein a data processing system can be applied to a DSC (page 1, lines 1-2). An advantage of the system taught by AAPA is the ability to make the system portable (page 1, lines 1-2). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Masuda and Reger to implement the data processing system in a DSC as taught by AAPA. Motivation to modify is to make the system portable.
- As per claim 12, AAPA teaches wherein a data processing system can be applied to a DVC (page 1, lines 1-2).
- As per claim 13, AAPA teaches wherein a data processing system can be applied to a digital voice recorder (page 1, lines 1-2).

- As per claim 14, AAPA teaches wherein a data processing system can be applied to an MP3 player (page 1, lines 1-2).

Response to Arguments

11. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anand Patel whose telephone number is (571) 272-7211. The examiner can normally be reached on Mon-Fri 8AM-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ABP

A. ELAMIN
PRIMARY EXAMINER